LISTING OF CLAIMS

The following listing of claims is provided as a convenience to the Examiner. No claim amendments are presented in this response.

1. (Original) A circuit for controlling the duty cycle and jitter of a clock signal, comprising:

an input node for receiving the clock signal; and

an output node for outputting a processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle.

2. (Original) A circuit as in claim 1, wherein said predetermined duty cycle is a nominally 50-50 duty cycle.

3. (Original) A circuit as in claim 1, wherein said output node is coupled to baseband circuitry of a wireless communications terminal.

4. (Original) A circuit as in claim1, and further comprising:

a plurality of serially connected delay elements that are coupled to said clock signal, said plurality of delay elements introducing a nominal one cycle delay into said clock signal;

a phase detector having a first input signal coupled to said clock signal and a second input coupled to an output of said plurality of delay elements for receiving a delayed clock signal therefrom, said phase detector operating so as to generate an error signal that is indicative of a phase difference between said clock signal and said delayed clock signal, said error signal being coupled to at least a first one of said delay elements for controlling said at least one delay element for minimizing the phase difference between said clock signal and said delayed clock signal;

a first divider circuit having an input coupled to said clock signal;

a second divider circuit having an input coupled to an output of said first one of said plurality of delay elements for receiving a one half cycle delayed clock signal therefrom; and

a gate having inputs coupled to outputs of said first and second divider circuits and an output coupled to said output node for outputting said processed clock signal.

5. (Original) A method for processing a clock signal, comprising:

providing a clock control circuit having an input node and an output node;

receiving the clock signal at the input node; and

outputting a processed clock signal from the output node, the processed clock signal having a first edge that is synchronized to an edge of the clock signal and a second edge that is varied so as to provide a predetermined processed clock signal duty cycle.

6. (Original) A method as in claim 5, wherein the predetermined duty cycle is a 50-50 duty cycle.

7. (Original) A method as in claim 5, wherein the output node is coupled to baseband circuitry of a wireless communications terminal.

8. (Original) A method as in claim 5, wherein the first edge of the processed clock signal is a rising edge that is synchronized to a rising edge of the clock signal.